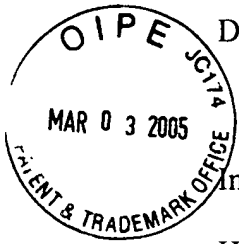


*JPW*



Docket No.: 57454-973

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Customer Number: 20277  
Hideto HIDAKA : Confirmation Number: 5812  
Application No.: 10/680,397 : Group Art Unit: 2815  
Filed: October 08, 2003 : Allowed: February 25, 2005  
Examiner: George C. Eckert, II

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE OPERATING WITH  
LOW POWER CONSUMPTION

**LETTER SUBMITTING FORMAL DRAWINGS**  
**AS REPLACEMENT SHEETS**

Mail Stop ISSUE FEE  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In response to the Notice of Allowability dated February 25, 2005, submitted herewith is One (1) sheet of Formal Drawings correcting Fig. 104, labeled as Replacement Sheet, in connection with the above referenced application.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

*Becker*  
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Registration No. 26,527

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**Date: March 3, 2005**

**Please recognize our Customer No. 20277  
as our correspondence address.**